AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below.

1. (Original) Apparatus comprising:

a branch prediction unit to predict whether a branch is to be taken;

an instruction fetch unit to fetch an instruction; and

a control circuit coupled to the branch prediction unit, wherein the control circuit is to abort the fetched instruction at a pre-decoding stage if the branch is predicted to be taken.

2. (Original) The apparatus of claim 1, further comprising:

an instruction length decoder, wherein the control circuit is to block data associated with the instruction from entering the instruction length decoder.

3. (Original) The apparatus of claim 1, further comprising:

an instruction length decoder, wherein the control circuit is to block processing of data associated with the instruction by the instruction length decoder.

4. (Original) The apparatus of claim 1, wherein the instruction fetch unit is to fetch a branch target if the branch prediction unit determines that the branch is predicted to be taken.

5. (Original) The apparatus of claim 1, wherein the branch prediction unit is to transmit a branch taken signal to the control circuit if the branch is predicted to be taken.

6. (Currently amended) The apparatus of claim 5, wherein the ~~power~~ control circuit is to prevent an output of a cache array to be input to an instruction length decoder in response to the branch taken signal.

7. (Currently amended) The apparatus of claim 1, wherein the fetched instruction is a next sequential instruction.

8. (Currently amended) A method comprising:

predicting whether a branch is to be taken;

fetching a next instruction;

terminating a process associated with the next ~~sequential~~ instruction if the branch is predicted to be taken.

9. (Currently amended) The method of claim 8, further comprising:

blocking data associated with the next ~~sequential~~ instruction from entering an instruction length decoder if the branch is predicted to be taken.

10. (Original) The method of claim 8, further comprising:

redirecting an instruction fetch unit to the predicted branch if the branch is predicted to be taken.

11. (Original) The method of claim 10, further comprising:

fetching a branch target by the instruction fetch unit if the branch is predicted to be taken.

12. (Original) The method of claim 8, further comprising:

transmitting a branch taken signal to a control circuit if the branch is predicted to be taken.

13. (Currently amended) The method of claim 12, further comprising:

terminating power for processes associated with the next ~~sequential~~ instruction if the branch signal is received.

14. (Original) An apparatus comprising:

means for predicting whether a branch is to be taken;

means for fetching a next sequential instruction; and

means coupled to the branch prediction unit for aborting the next sequential instruction if the branch is predicted to be taken.

15. (Original) The apparatus of claim 14, comprises:

means for preventing information associated with the next sequential instruction from being sent to an instruction length decoder if the branch is predicted to be taken.

16. (Currently amended) A system comprising:

a bus;

an external memory coupled to the bus; and

a processor coupled to the bus, the processor including:

a branch prediction unit to predict whether a branch is to be taken;

a instruction fetch unit to fetch a next ~~sequential~~ instruction; and

a control circuit coupled to the branch prediction unit, the control circuit to abort the next ~~sequential~~ instruction if the branch is predicted to be taken.

17. (Original) The system of claim 16, wherein the bus is a PCI bus.

18. (Original) The system of claim 16, wherein the bus is an ISA bus.

19. (Original) The system of claim 16, wherein the external memory is a SRAM.

20. (Original) The system of claim 16, wherein the external memory is a DRAM.

21. (Original) The system of claim 16, the processor further including:

an instruction length decoder, wherein the control circuit is to block data associated with the next instruction from entering the instruction length decoder.

22. (Original) The system of claim 16, the processor further including:

an instruction length decoder, wherein the control circuit is to block processing of data associated with the next instruction by the instruction length decoder.

23. (Original) The system of claim 16, wherein the instruction fetch unit is to fetch a branch target if the branch prediction unit determines that the branch is predicted to be taken.

24. (Original) The system of claim 16, wherein the branch prediction unit is to transmit a branch taken signal to the control circuit if the branch is predicted to be taken.

25. (Currently amended) The system of claim 24, wherein the ~~power~~ control circuit is to prevent an output of a cache array to be input to an instruction length decoder in response to the branch taken signal.

26. (Original) The system of claim 16, wherein the next instruction is a next sequential instruction.

27. (Currently amended) Apparatus comprising:

an instruction pointer to fetch a next sequential instruction for processing;

an instruction cache array coupled to the instruction pointer to output information associated with the next sequential instruction;

a latch coupled between the output of the instruction cache array and a instruction length decoder;

a circuit to open the latch to prevent the information associated with the next sequential instruction from being output to the instruction length decoder if a branch taken signal is received, wherein the branch taken signal indicates that a branch has been predicted to be taken.

28. (Currently amended) The apparatus of claim 27, the circuit comprising:

an AND gate having a first input, second input and an output, wherein the first input is an inverted branch taken signal and the second input is an inverted clock and the output is used to open the latch ~~to prevent the information associated with the next sequential instruction from being output to the instruction length decoder if the branch is predicted to be taken~~.

29. (Original) An apparatus comprising:

an instruction pointer to fetch a next sequential instruction for processing;

a branch prediction unit to determine that a branch is to be taken and generate a branch taken signal;

a cache logic array coupled to the instruction pointer to receive data associated with the next sequential instruction and to receive the branch taken signal;

an instruction length decoder coupled to the cache logic array, wherein responsive to the received branch taken signal, the cache logic array is to abort further processing of the data associated with the next sequential instruction.

30. (Original) The apparatus of claim 29, further comprising:

circuitry to block the data associated with the next sequential instruction from entering the instruction length decoder if the branch taken signal is received.